128K x 36, 256K x 18 3.3V Synchronous SRAMs 3.3V I/O, Pipelined Outputs Burst Counter, Single Cycle Deselect

IDT71V35761S
IDT71V35781S
IDT71V35761SA
IDT71V35781SA

Features

- **128K x 36, 256K x 18 memory configurations**
- **Supports high system speed:**
  Commercial:
  – *200MHz 3.1ns clock access time*
  Commercial and Industrial:
  – *183MHz 3.3ns clock access time*
  – *166MHz 3.5ns clock access time*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **3.3V I/O**
- **Optional - Boundary Scan JTAG Interface (IEEE 1149.1 compliant)**
- **Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array**

Description

The IDT71V35761/781 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V35761/781 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V35761/81 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V35761/781 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array.

Pin Description Summary

A_0-A_{17}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
TMS	Test Mode Select	Input	Synchronous
TDI	Test Data Input	Input	Synchronous
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	Synchronous
$\overline{TRST}$	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

5301 tbl 01

NOTE:
1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V35781.

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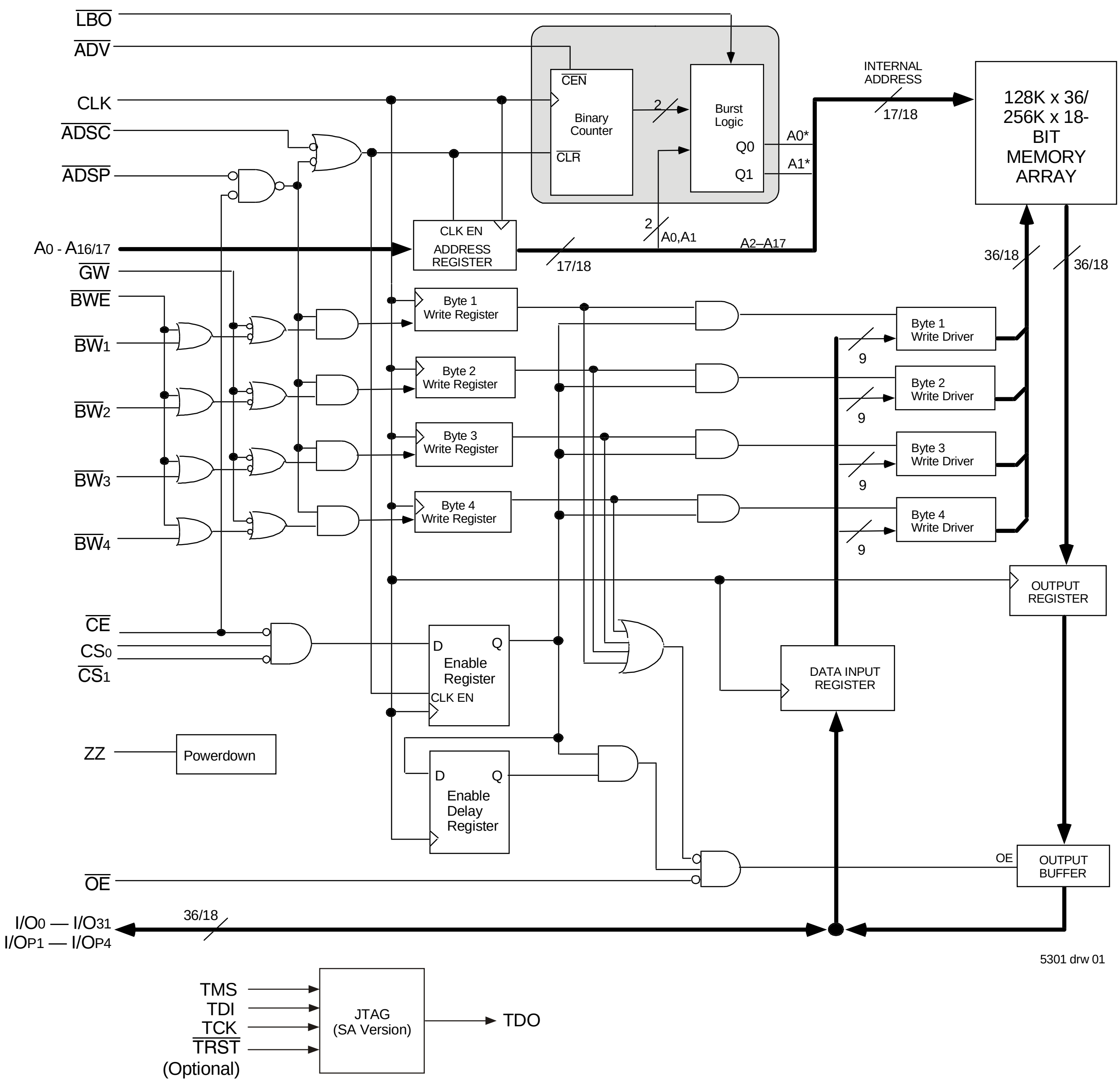
Pin Definitions[(1)]

Symbol	Pin Function	I/O	Active	Description
A_0-A_{17}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low.
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{\text{ADSP}}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$.
$\overline{\text{ADV}}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{\text{BWE}}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{\text{BW}}_1$-$\overline{\text{BW}}_4$. If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BW}}_x$ inputs are passed to the next stage in the circuit. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle.
$\overline{\text{BW}}_1$-$\overline{\text{BW}}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{\text{BW}}_1$ controls I/O_{0-7}, I/O_{P1}, $\overline{\text{BW}}_2$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{\text{CE}}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{\text{CE}}$ is used with CS_0 and $\overline{\text{CS}}_1$ to enable the IDT71V35761/781. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{\text{CE}}$ and $\overline{\text{CS}}_1$ to enable the chip.
$\overline{\text{CS}}_1$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{\text{CS}}_1$ is used with $\overline{\text{CE}}$ and CS_0 to enable the chip.
$\overline{\text{GW}}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{\text{LBO}}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{\text{LBO}}$ is HIGH, the interleaved burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear burst sequence is selected. $\overline{\text{LBO}}$ is a static input and must not change state while the device is operating.
$\overline{\text{OE}}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state.
TMS	Test ModeSelect	I	N/A	Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.
TDO	Test DataOutput	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
$\overline{\text{TRST}}$	JTAG Reset (Optional)	I	LOW	Optional Asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used $\overline{\text{TRST}}$ can be left floating. This pin has an internal pullup. Only available in BGA package.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V35761/35781 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.This pin has an internal pull down.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.

5301tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A[7]	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5301 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5301 tbl 04

NOTES:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3[1]	V
V_{IL}	Input Low Voltage	-0.3[2]	—	0.8	V

5301 tbl 06

NOTES:
1. V_{IH} (max) = VDDQ + 1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100 Pin TQFP Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5301 tbl 07

119 BGA Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5301 tbl 07a

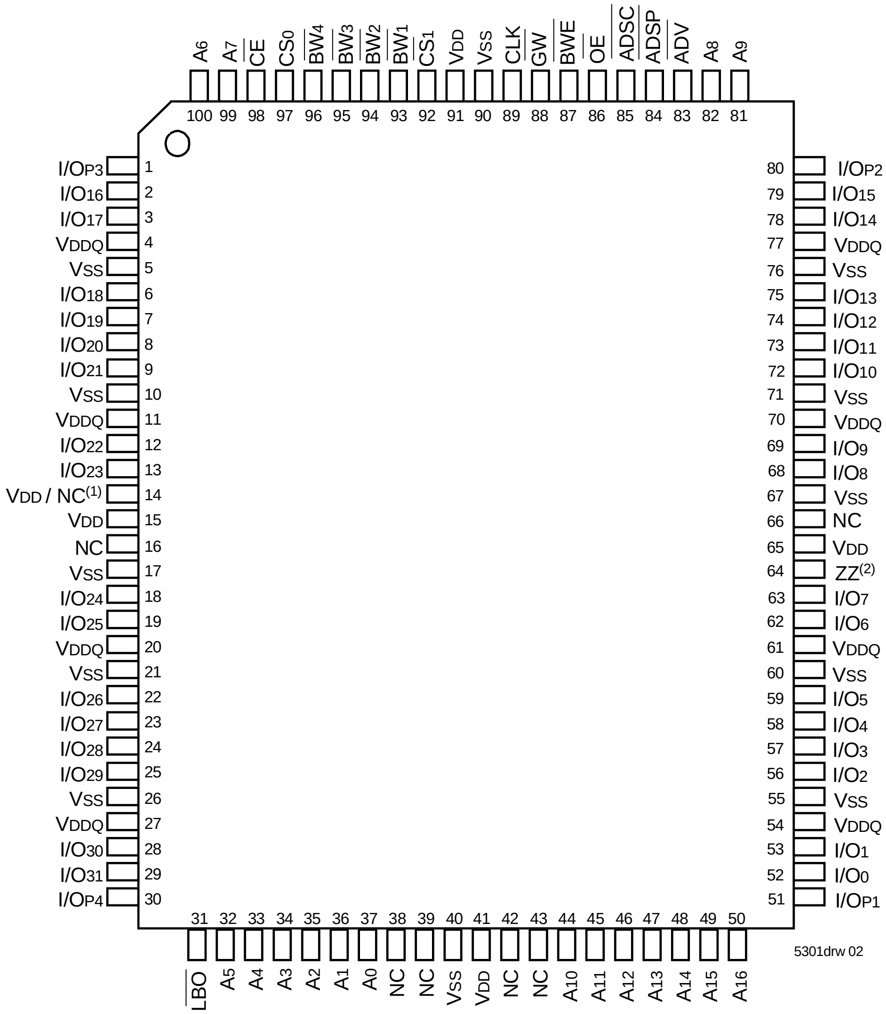
165 fBGA Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5301 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

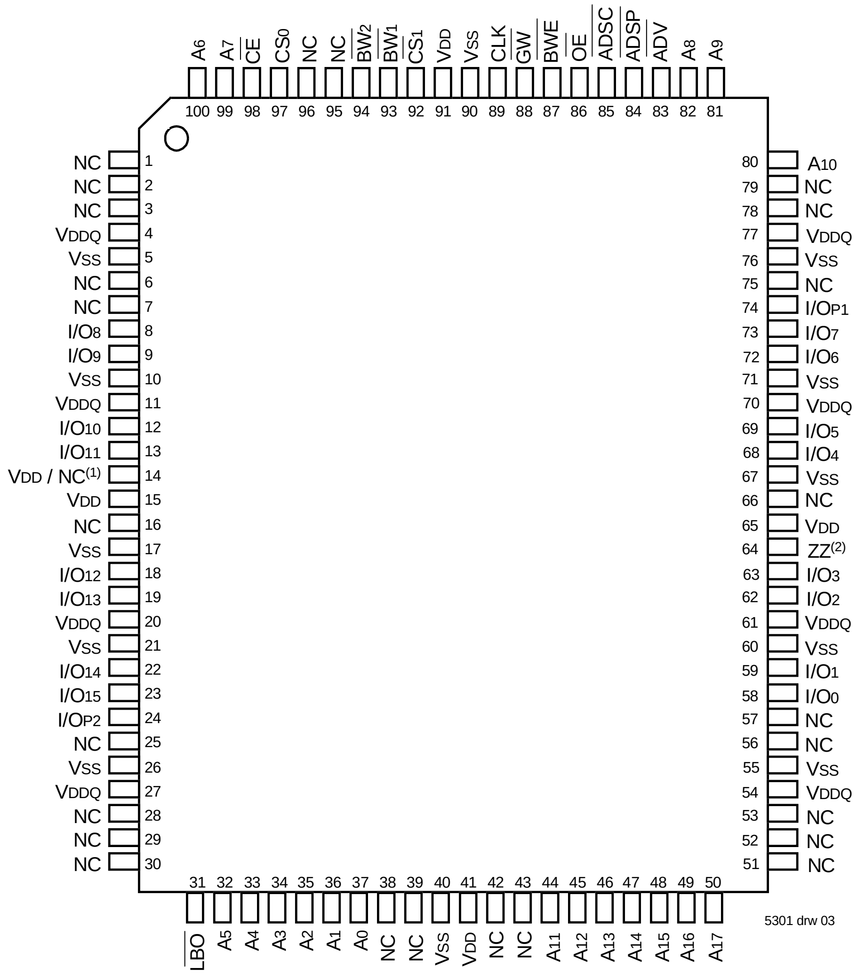
Pin Configuration – 128K x 36



100 TQFP
Top View

NOTES:
1. Pin 14 can either be directly connected to V_{DD}, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 256K x 18



100 TQFP
Top View

NOTES:

1. Pin 14 can either be directly connected to V_{DD}, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 128K x 36, 119 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{DDQ}
B	NC	CS0	A3	$\overline{ADSC}$	A9	$\overline{CS1}$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O16	I/OP3	V_{SS}	NC	V_{SS}	I/OP2	I/O15
E	I/O17	I/O18	V_{SS}	$\overline{CE}$	V_{SS}	I/O13	I/O14
F	V_{DDQ}	I/O19	V_{SS}	$\overline{OE}$	V_{SS}	I/O12	V_{DDQ}
G	I/O20	I/O21	$\overline{BW3}$	$\overline{ADV}$	$\overline{BW2}$	I/O11	I/O10
H	I/O22	I/O23	V_{SS}	$\overline{GW}$	V_{SS}	I/O9	I/O8
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	I/O24	I/O26	V_{SS}	CLK	V_{SS}	I/O6	I/O7
L	I/O25	I/O27	$\overline{BW4}$	NC	$\overline{BW1}$	I/O4	I/O5
M	V_{DDQ}	I/O28	V_{SS}	$\overline{BWE}$	V_{SS}	I/O3	V_{DDQ}
N	I/O29	I/O30	V_{SS}	A1	V_{SS}	I/O2	I/O1
P	I/O31	I/OP4	V_{SS}	A0	V_{SS}	I/O0	I/OP1
R	NC	A5	$\overline{LBO}$	V_{DD}	V_{DD} / NC[1]	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ[3]
U	V_{DDQ}	NC/TMS[2]	NC/TDI[2]	NC/TCK[2]	NC/TDO[2]	NC/$\overline{TRST}$[2,4]	V_{DDQ}

5301 drw 04

Top View

Pin Configuration – 256K x 18, 119 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{DDQ}
B	NC	CS0	A3	$\overline{ADSC}$	A9	$\overline{CS1}$	NC
C	NC	A7	A2	V_{DD}	A13	A17	NC
D	I/O8	NC	V_{SS}	NC	V_{SS}	I/O7	NC
E	NC	I/O9	V_{SS}	$\overline{CE}$	V_{SS}	NC	I/O6
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	I/O5	V_{DDQ}
G	NC	I/O10	$\overline{BW2}$	$\overline{ADV}$	V_{SS}	NC	I/O4
H	I/O11	NC	V_{SS}	$\overline{GW}$	V_{SS}	I/O3	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	I/O12	V_{SS}	CLK	V_{SS}	NC	I/O2
L	I/O13	NC	V_{SS}	NC	$\overline{BW1}$	I/O1	NC
M	V_{DDQ}	I/O14	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	I/O15	NC	V_{SS}	A1	V_{SS}	I/O0	NC
P	NC	I/OP2	V_{SS}	A0	V_{SS}	NC	I/OP1
R	NC	A5	$\overline{LBO}$	V_{DD}	V_{DD} / NC[1]	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ[3]
U	V_{DDQ}	NC/TMS[2]	NC/TDI[2]	NC/TCK[2]	NC/TDO[2]	NC/$\overline{TRST}$[2,4]	V_{DDQ}

5301 drw 05

Top View

NOTES:

1. R5 can either be directly connected to V_{DD}, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version. Note: If NC, these pins can either be tied to V_{SS}, V_{DD} or left floating.
3. T7 can be left unconnected and the device will always remain in active mode.
4. $\overline{TRST}$ is offered as an optional JTAG Reset if required in the application. If not needed, can be left floating and will internally be pulled to V_{DD}.

Pin Configuration – 128K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(4)	A7	$\overline{CE}_1$	$\overline{BW}_3$	$\overline{BW}_2$	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	NC
B	NC	A6	CS0	$\overline{BW}_4$	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(4)
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VDD(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(3)
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	NC/$\overline{TRST}$(2,5)	NC(4)	NC	VSS	VDDQ	NC	I/OP1
P	NC	NC(4)	A5	A2	NC/TDI(2)	A1	NC/TDO(2)	A10	A13	A14	NC(4)
R	$\overline{LBO}$	NC(4)	A4	A3	NC/TMS(2)	A0	NC/TCK(2)	A11	A12	A15	A16

5301 tbl 17

Pin Configuration – 256K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(4)	A7	$\overline{CE}_1$	$\overline{BW}_2$	NC	$\overline{CS}_1$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	A10
B	NC	A6	CS0	NC	$\overline{BW}_1$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(4)
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VDD(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(3)
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	NC/$\overline{TRST}$(2,5)	NC(4)	NC	VSS	VDDQ	NC	NC
P	NC	NC(4)	A5	A2	NC/TDI(2)	A1	NC/TDO(2)	A11	A14	A15	NC(4)
R	$\overline{LBO}$	NC(4)	A4	A3	NC/TMS(2)	A0	NC/TCK(2)	A12	A13	A16	A17

5301 tbl 17a

NOTES:
1. H1 can either be directly connected to VDD, or connected to an input voltage ≥ VIH, or left unconnected.
2. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version. Note: If NC, these pins can either be tied to VSS, VDD or left floating.
3. H11 can be left unconnected and the device will always remain in active mode.
4. Pins P11, N6, B11, A1, R2 and P2 are reserved for 9M, 18M, 36M, 72M, 144M and 288M respectively.
5. $\overline{TRST}$ is offered as an optional JTAG Reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\lvert I_{LZZ} \rvert$	ZZ, $\overline{LBO}$ and JTAG Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5301 tbl 08

NOTE:
1. The $\overline{LBO}$, TMS, TDI, TCK & $\overline{TRST}$ pins will be internally pulled to V_{DD} and the ZZ pin will be internally pulled to V_{SS} if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

Symbol	Parameter	Test Conditions	200MHz	183MHz		166 MHz		Unit
			Com'l	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	360	340	350	320	330	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	30	30	35	30	35	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}(2,3)	130	120	130	110	120	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	30	30	35	30	35	mA

5301 tbl 09

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 3.3V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5301 tbl 10

AC Test Load

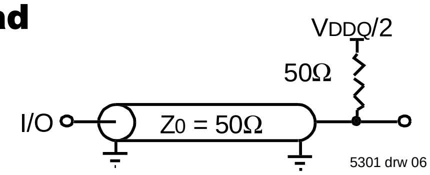


Figure 1. AC Test Load

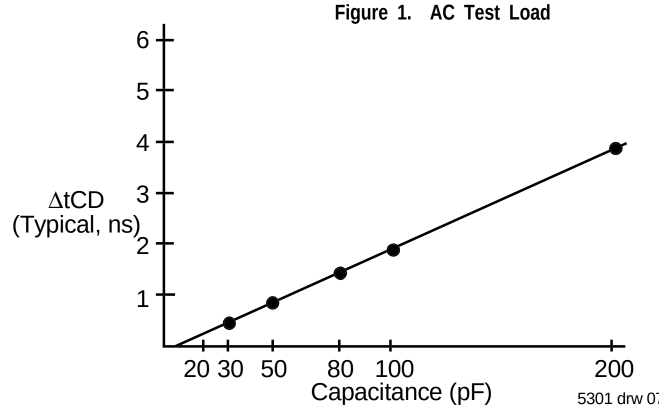


Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table[1,3]

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_x}$	$\overline{OE}$ (2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	-	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	-	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	-	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	-	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	-	D_{IN}
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	-	D_{IN}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	-	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	-	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	-	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	-	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	-	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	-	D_{IN}
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	-	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	-	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	-	D_{IN}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	-	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	-	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	-	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	-	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	-	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	-	D_{IN}
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	-	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	-	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	-	D_{IN}

5301tbl 11

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ = low for this table.

Synchronous Write Function Truth Table(1, 2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1(3)	H	L	L	H	H	H
Write Byte 2(3)	H	L	H	L	H	H
Write Byte 3(3)	H	L	H	H	L	H
Write Byte 4(3)	H	L	H	H	H	L

5301 tbl 12

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V35781.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5301 tbl 13

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5301 tbl 14

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5301 tbl 15

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

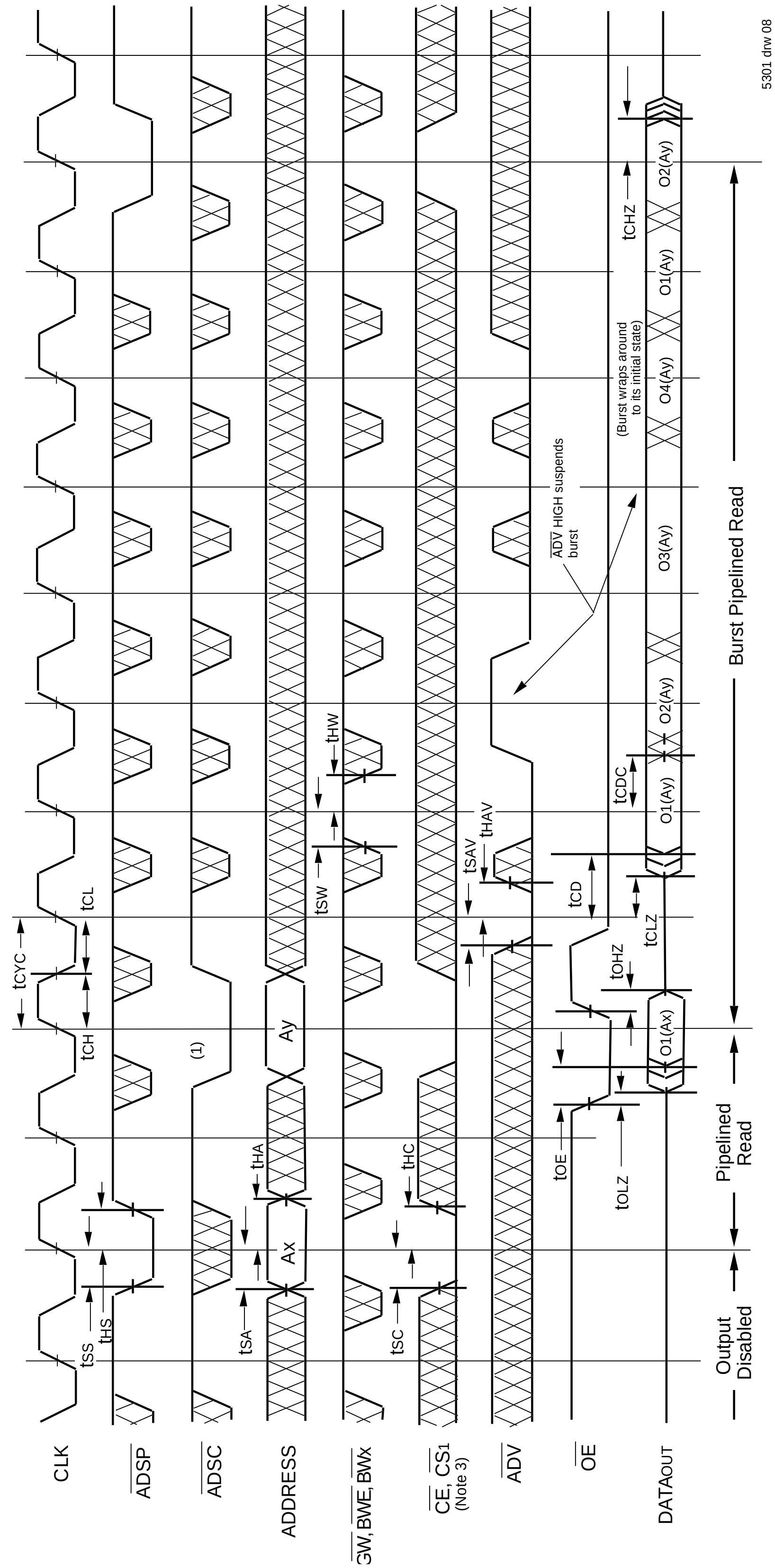
AC Electrical Characteristics
(V_{DD} = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	200MHz(5)		183MHz		166MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5	—	5.5	—	6	—	ns
t_{CH}(1)	Clock High Pulse Width	2	—	2.2	—	2.4	—	ns
t_{CL}(1)	Clock Low Pulse Width	2	—	2.2	—	2.4	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.1	—	3.3	—	3.5	ns
t_{CDC}	Clock High to Data Change	1.0	—	1.0	—	1.0	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	1.5	3.1	1.5	3.3	1.5	3.5	ns
t_{OE}	Output Enable Access Time	—	3.1	—	3.3	—	3.5	ns
t_{OLZ}(2)	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Output High-Z	—	3.1	—	3.3	—	3.5	ns
Set Up Times								
t_{SA}	Address Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SD}	Data In Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SW}	Write Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SAV}	Address Advance Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.2	—	1.5	—	1.5	—	ns
Hold Times								
t_{HA}	Address Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.4	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	20	—	22	—	24	—	ns

5301tbl 16

NOTES:
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.
5. Commercial temperature range only.

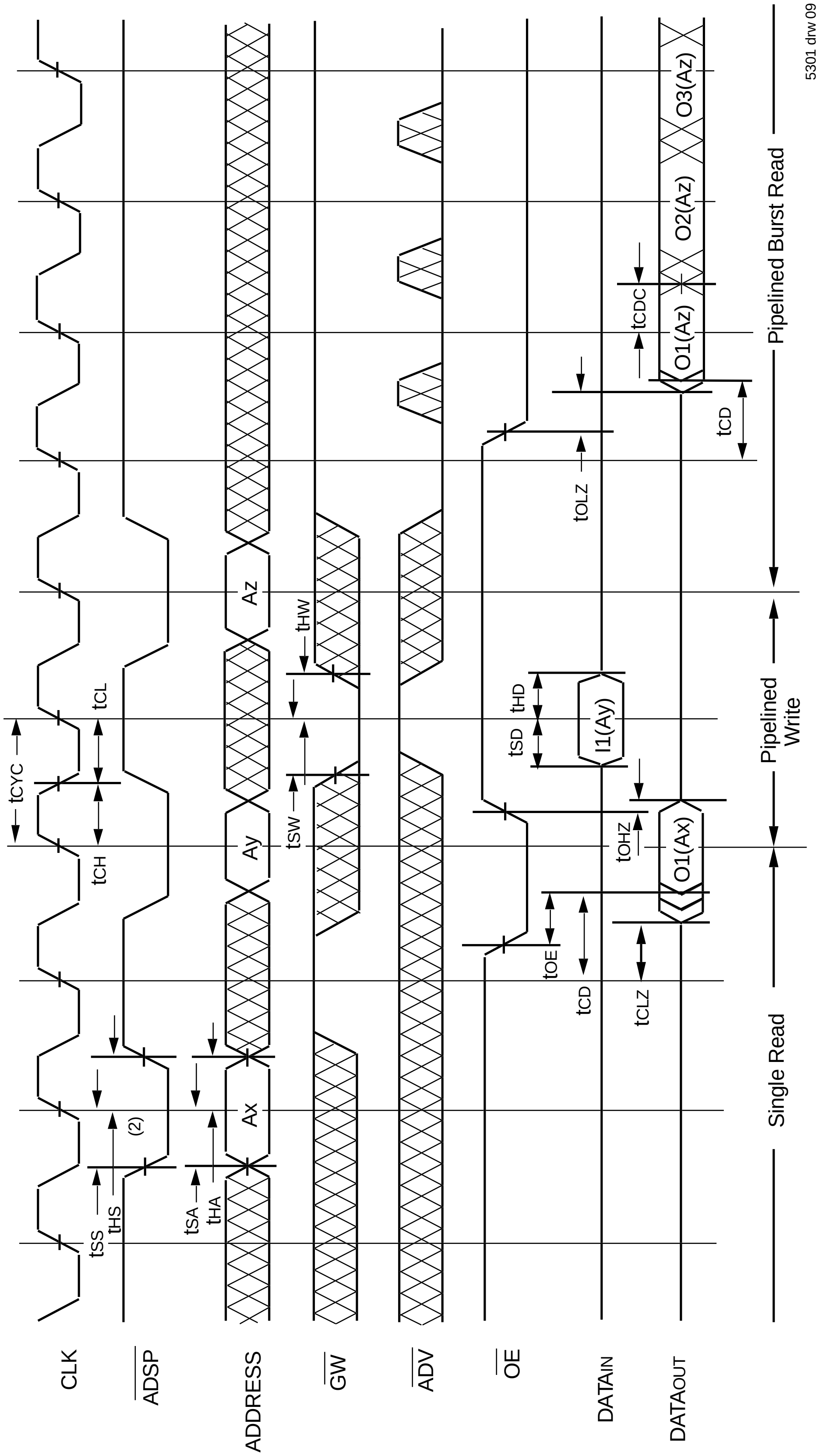
Timing Waveform of Pipelined Read Cycle[1,2]



NOTES:

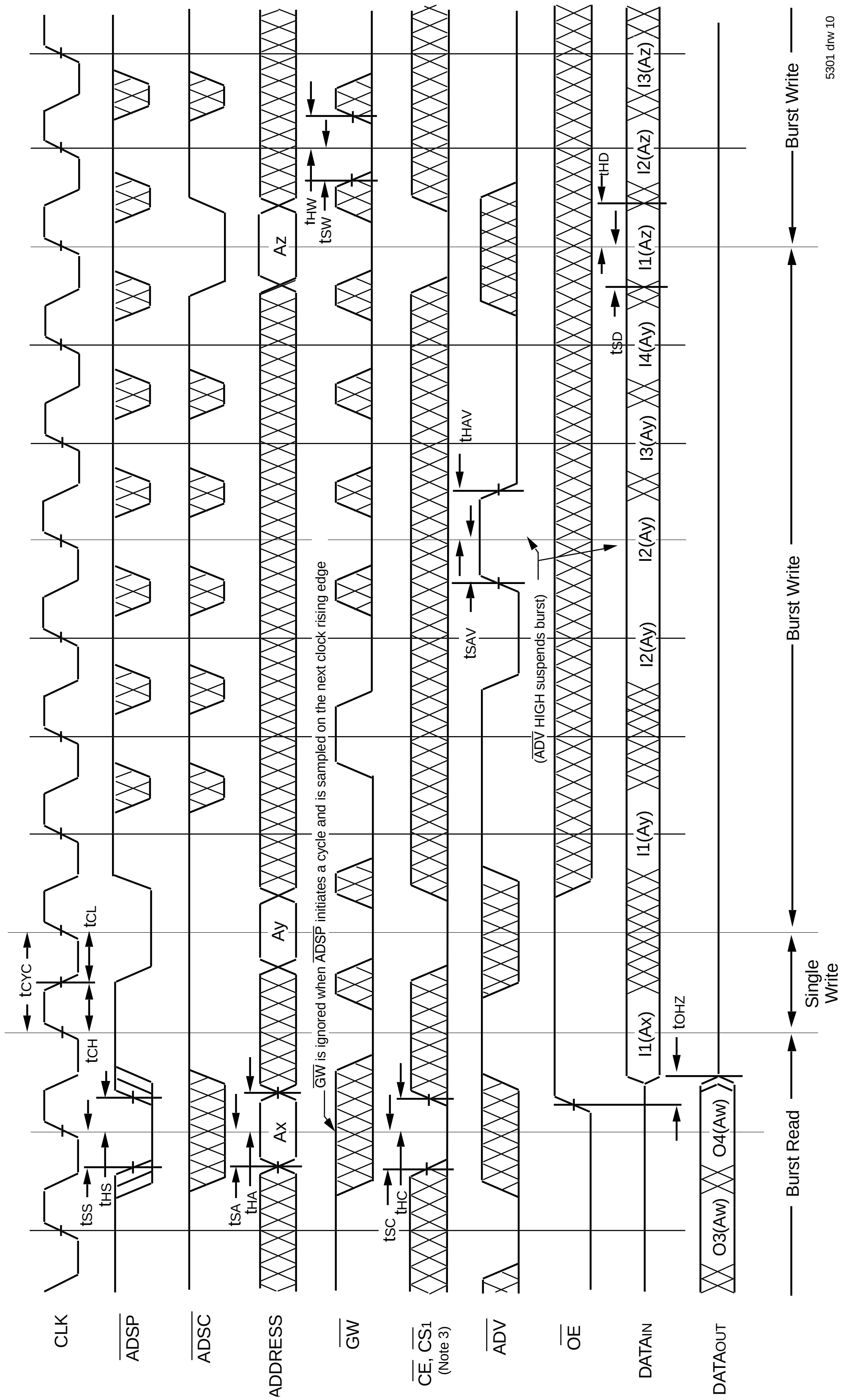
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Combined Pipelined Read and Write Cycles(1,2,3)



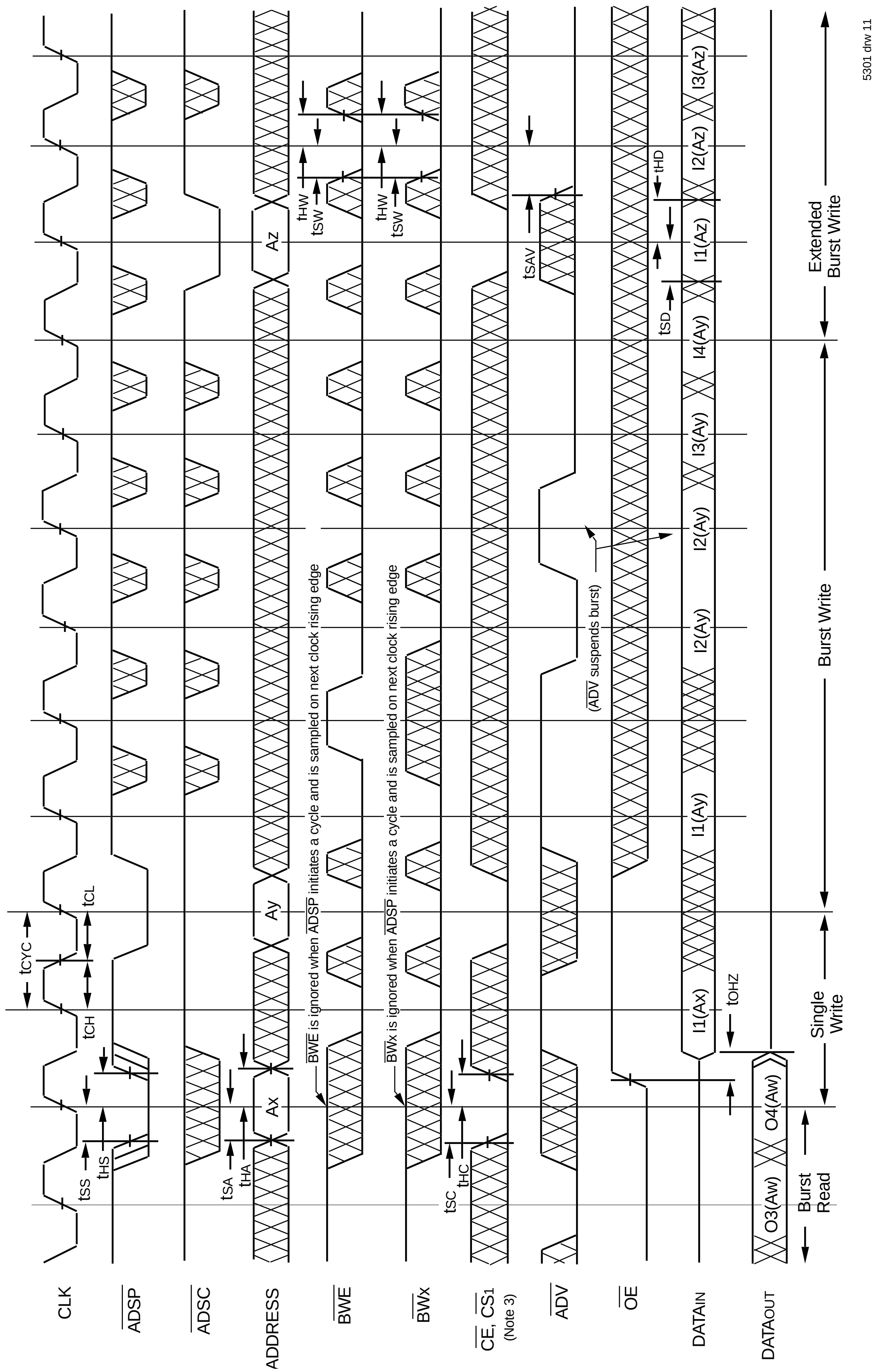
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS1}$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

Timing Waveform of Write Cycle No. 1 - $\overline{GW}$ Controlled(1,2,3)



NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

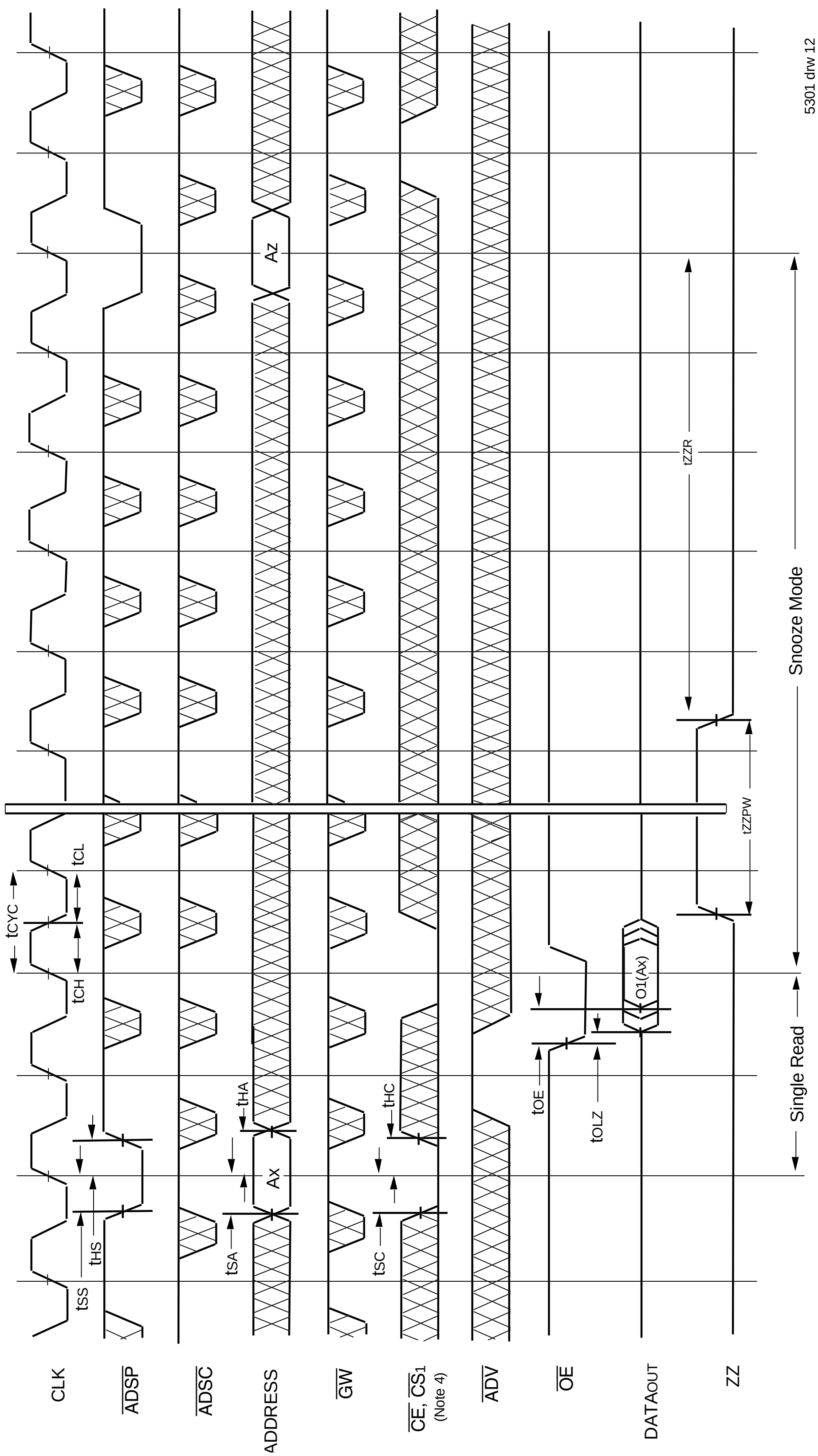
Timing Waveform of Write Cycle No. 2 - Byte Controlled(1,2,3)



NOTES:

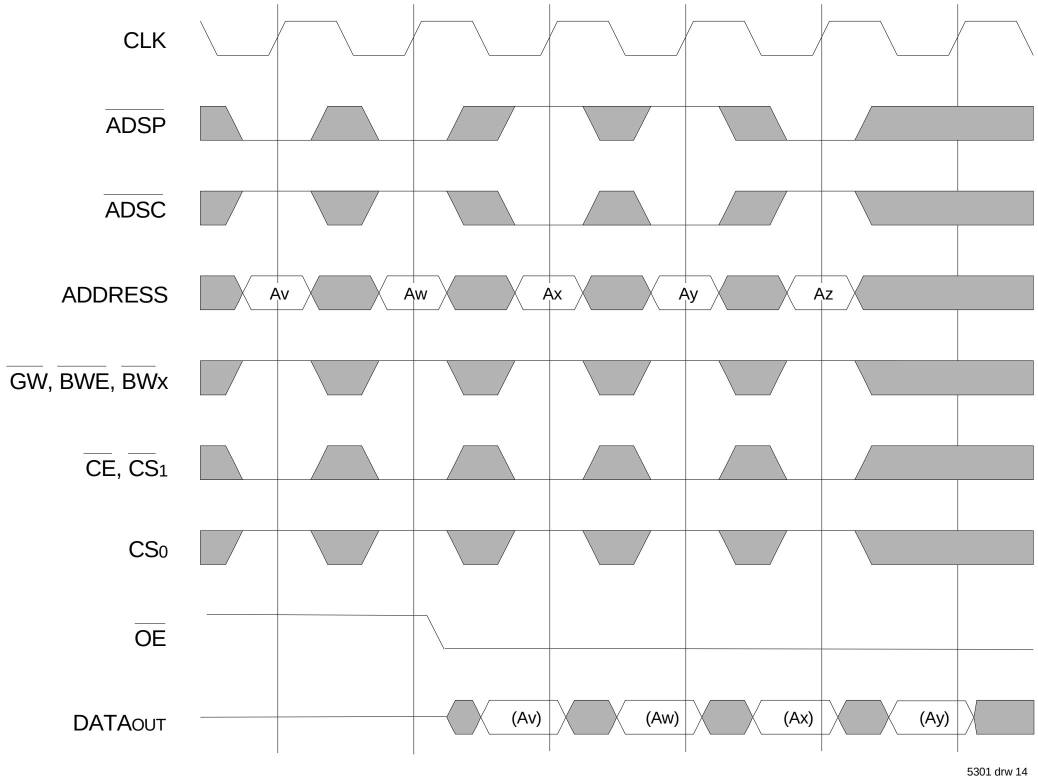
1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes(1,2,3)



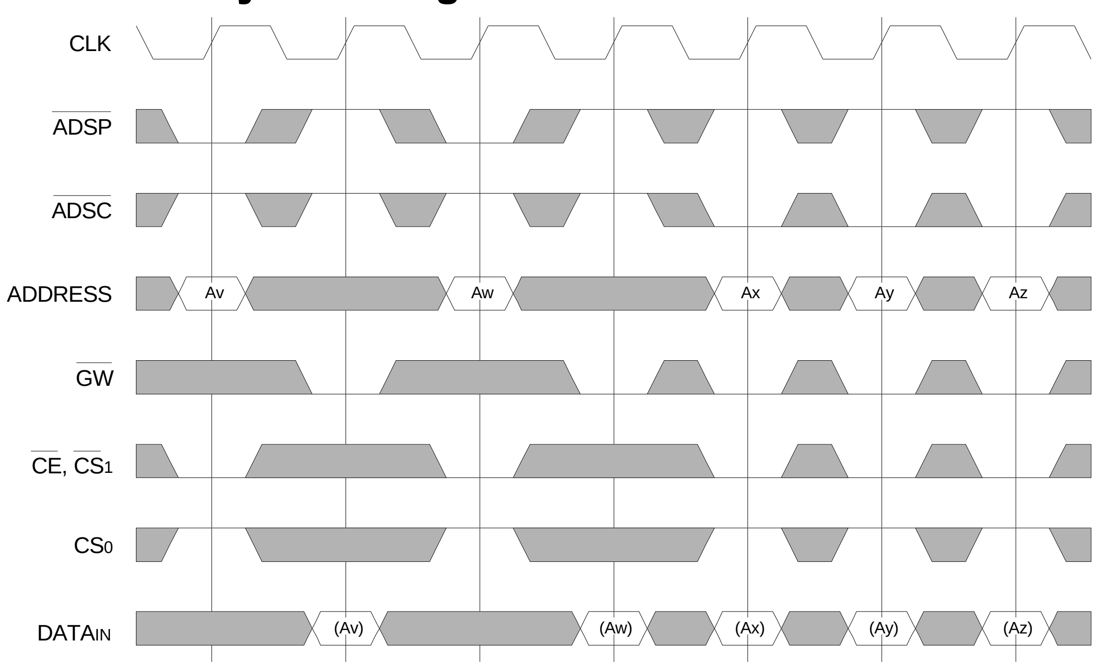
NOTES:
1. Device must power up in deselected Mode
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when CE and CS1 are LOW on this waveform, CS_0 is HIGH.

Non-Burst Read Cycle Timing Waveform



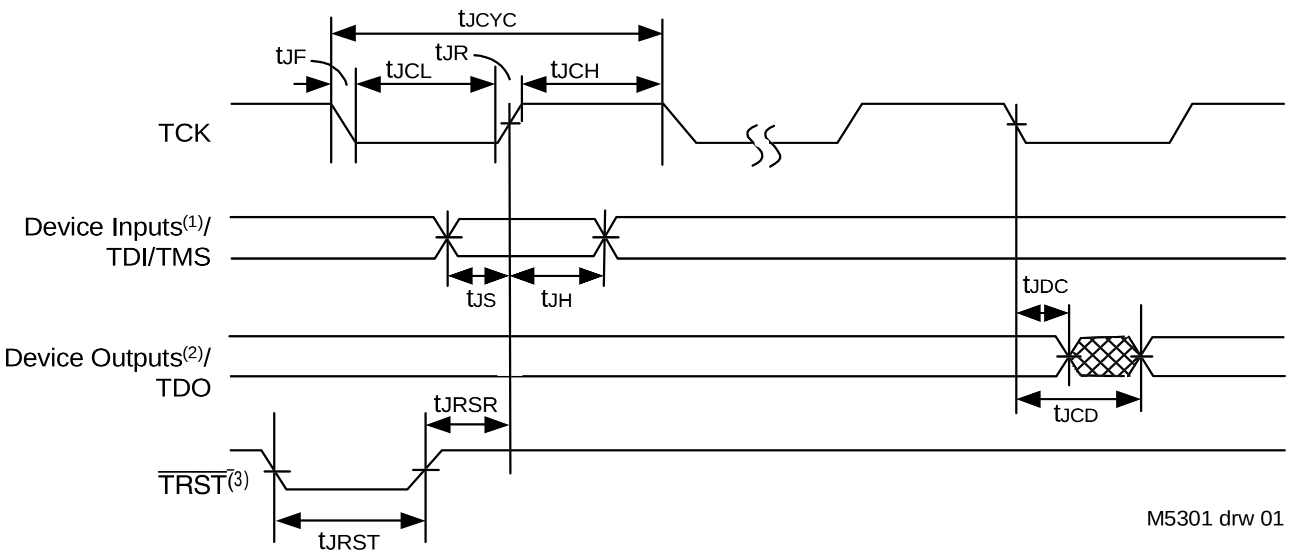
NOTES:
1. ZZ input is LOW, ADV is HIGH and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, ADSP and ADSC function identically and are therefore interchangable.

Non-Burst Write Cycle Timing Waveform



NOTES:
1. ZZ input is LOW, ADV and OE are HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only GW writes are shown, the functionality of BWE and BWx together is the same as GW.
4. For write cycles, ADSP and ADSC have different limitations.

JTAG Interface Specification (SA Version only)



NOTES:
1. Device inputs = All device inputs except TDI, TMS and TRST.
2. Device outputs = All device outputs except TDO.
3. During power up, TRST could be driven low or not be used since the JTAG circuit resets automatically. TRST is an optional JTAG reset.

JTAG AC Electrical Characteristics[1,2,3,4]

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5[1]	ns
t_{JF}	JTAG Clock Fall Time	—	5[1]	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

I5301 tbl 01

NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

I5301 tbl 03

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x23C, 0x23E	Defines IDT part number 71V35761SA and 71V35781SA, respectively.
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

I5301 tbl 02

Available JTAG Instructions

Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) and outputs(1) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

I5301 tbl 04

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.

Ordering Information

IDT XXX (Device Type) X S (Power) X (Speed) XX (Package) X (Process/ Temperature Range)

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	I	Industrial (-40°C to +85°C)
Package	PF**	100-pin Plastic Thin Quad Flatpack (TQFP)
	BG	119 Ball Grid Array (BGA)
	BQ	165 Fine Pitch Ball Grid Array (fBGA)
Speed	200*	Frequency in Megahertz
	183	
	166	
Power	S	Standard Power
	SA	Standard Power with JTAG interface
X	Blank	First Generation or current stepping
	Y	Second Generation die step
Device Type	71V35761	128K x 36 Pipelined Burst Synchronous SRAM with 3.3V I/O
	71V35781	256K x 18 Pipelined Burst Synchronous SRAM with 3.3V I/O

*Commercial temperature range only
** JTAG (SA version) is not available with 100 pin TQFP package.

5301 drw 13

Package Information

100-Pin Thin Quad Plastic Flatpack (TQFP)
119 Ball Grid Array (BGA)
165 Fine Pitch Ball Grid Array (fBGA)
Information available on the IDT website

Datasheet Document History

12/31/99		Created new datasheet from 71v3576 and 71v3578 datasheet.
	Pg. 1, 4, 8, 11, 19	Added industrial temperature range offering from 166MHz and 183MHz
04/04/00	Pg. 18	Added 100 pin TQFP package Diagram Outline
	Pg. 4	Add BGA capacitance table; Add industrial tempertaure to table; Insert note to Absolute Max Rating and Recommended Operating Temperature tables
06/01/00		Add new package diagram outline, 13 x 15mm 165fBGA
	Pg. 20	Correct BG119 Package Diagram Outline
07/15/00	Pg. 7	Add note reference to BG119 pinout
	Pg. 8	Add DNU reference note to BQ165 pinout
	Pg. 20	Update BG119 Package Diagram Outline Dimensions
10/25/00		Remove Preliminary status
	Pg. 8	Add reference note to N5 on the BQ165 pinout, reserved for JTAG $\overline{TRST}$
04/22/03	Pg.4	Updated 165 BGA table information from TBD to 7
06/30/03	Pg. 1,2,3,5-9	Updated datasheet with JTAG information
	Pg. 5-8	Removed note for NC pins (38,39(PF package); L4, U4 (BG package) H2, N7 (BQ package)) requiring NC or connection to Vss.
	Pg. 19,20	Added two pages of JTAG Specification, AC Electrical, Definitions and Instructions
	Pg. 21-23	Removed old package information from the datasheet
	Pg. 24	Updated ordering information with JTAG and Y stepping information. Added information regarding packages available IDT website.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800-544-7726, x4033

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